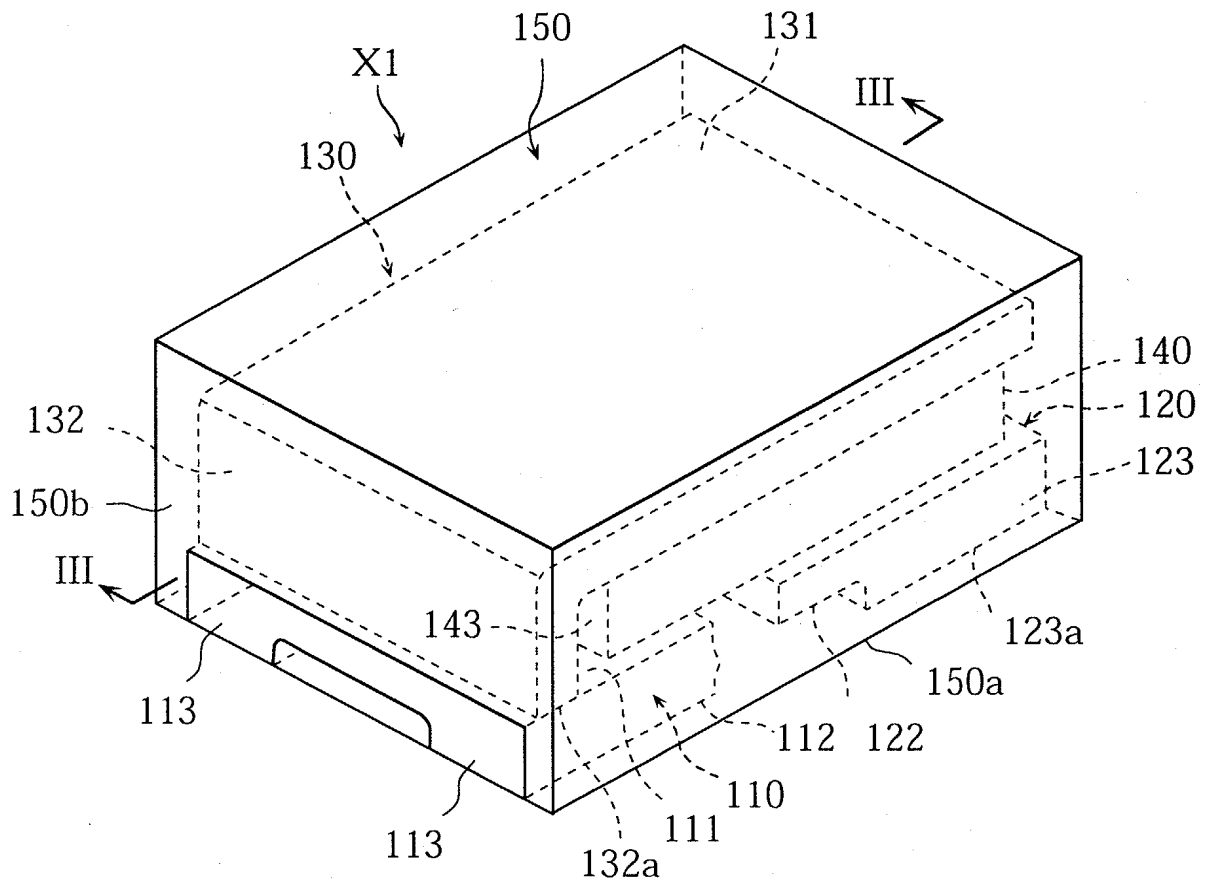


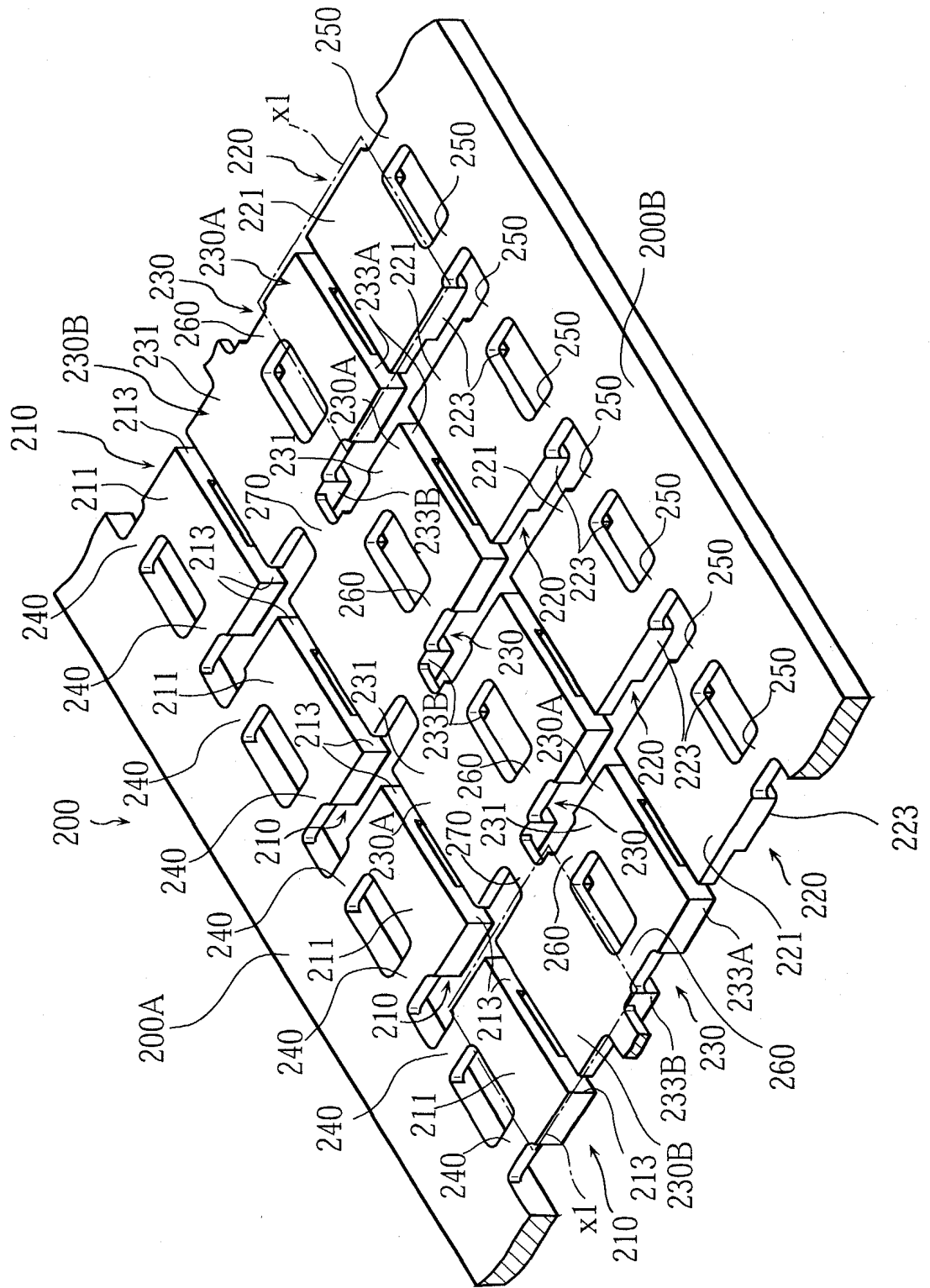
FIG. 1



[illegible]

This cross-sectional view shows the device structure along line X1-X1. It features a substrate 110 with a top layer 111. A gate stack 130 is formed on the substrate, consisting of a gate dielectric 131 and a gate electrode 132. The gate electrode 132 is divided into a central region 131a and side regions 132a. A channel layer 140 is located beneath the gate electrode 132, with a channel region 141 under the central gate and a channel extension region 142 under the side gates. Source and drain regions 120 are formed on the substrate, with a source region 121 and a drain region 122. The source region 121 is divided into a central part 122a and a side part 123. A source/drain extension layer 150 is formed on the channel extension region 142 and the source/drain regions 120, with a central part 150a and side parts 150b. The side parts 150b are located under the side gate regions 132a. The device is surrounded by a passivation layer 113, which has a top surface 113a.

FIG. 4



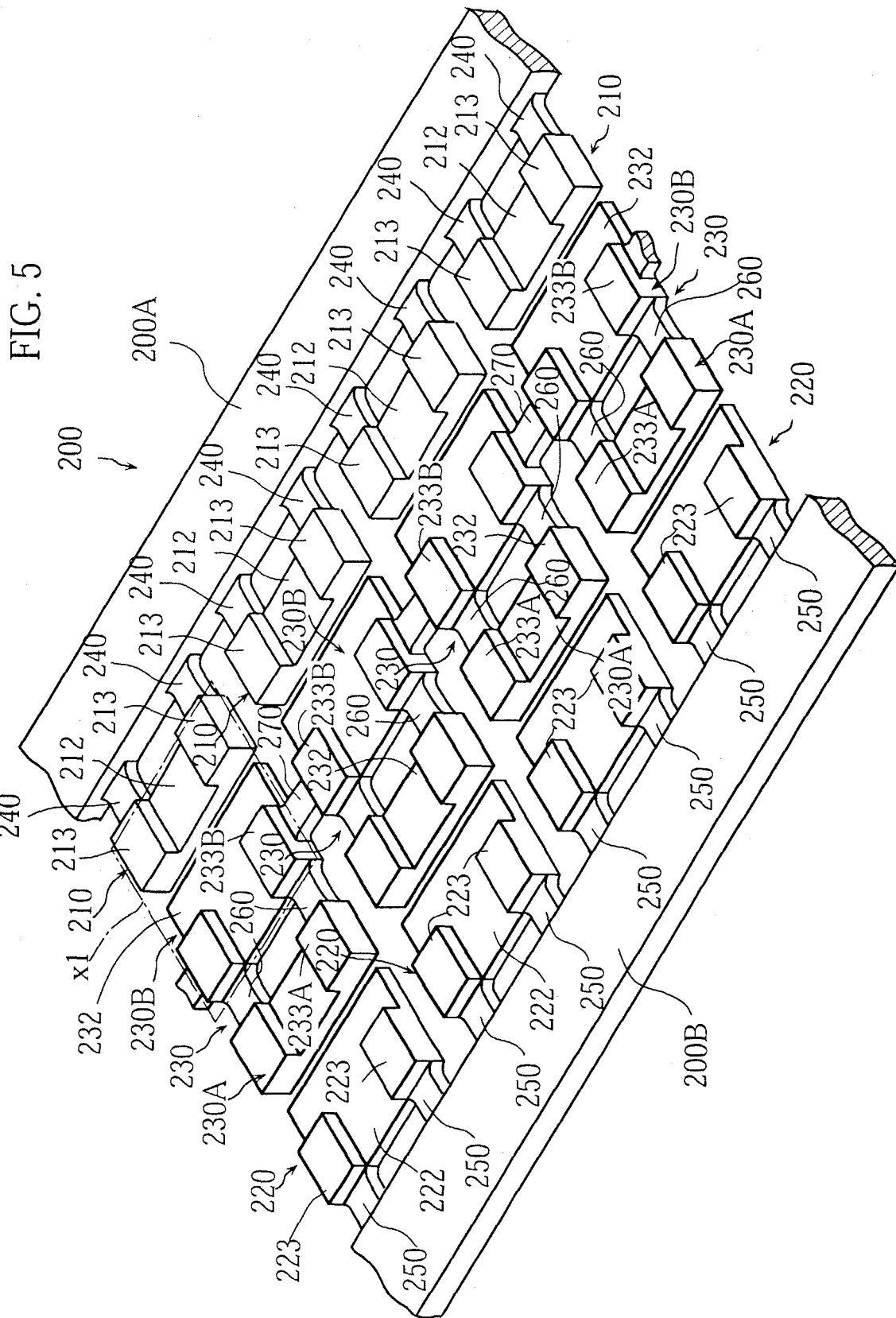


FIG. 6

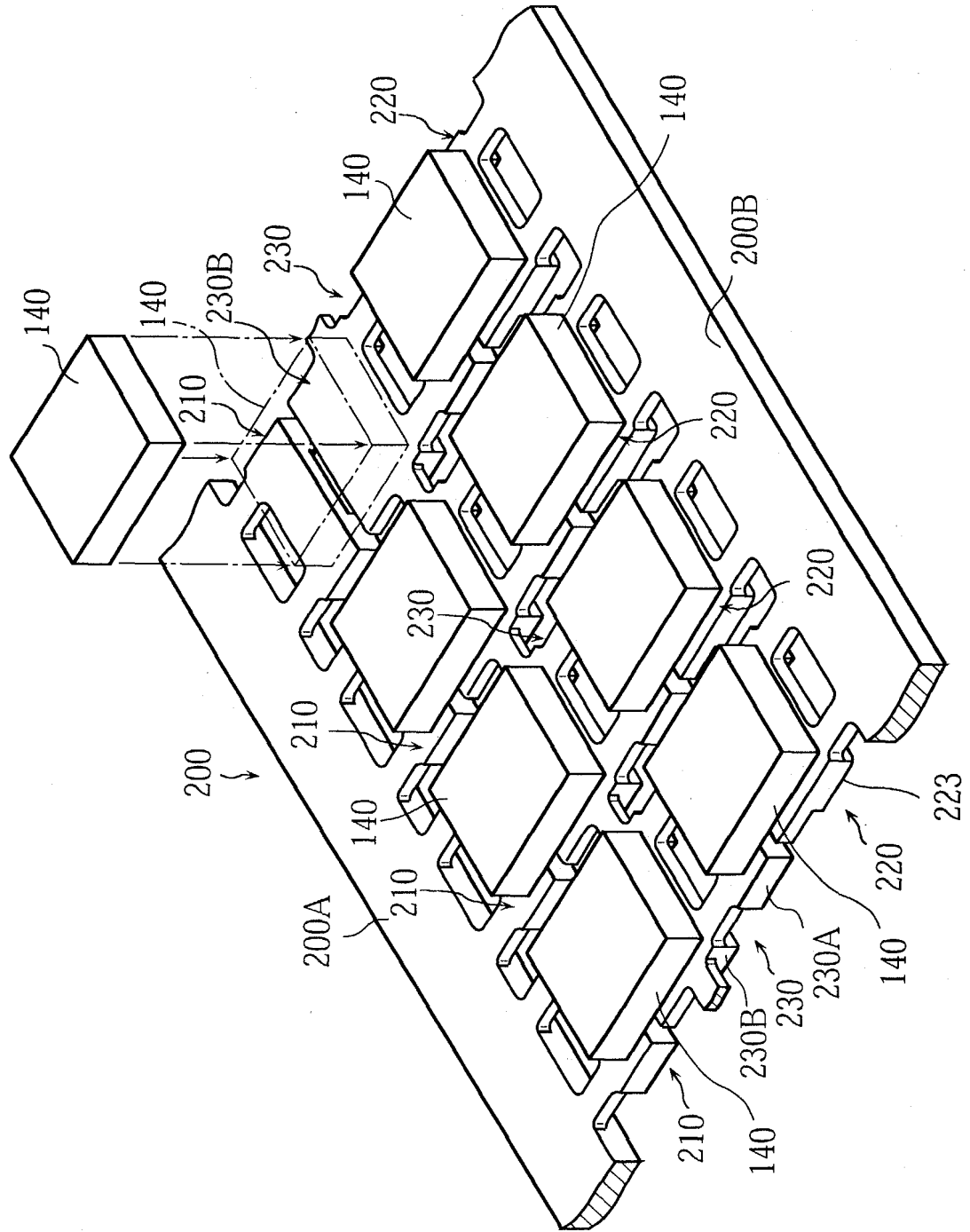


FIG. 7

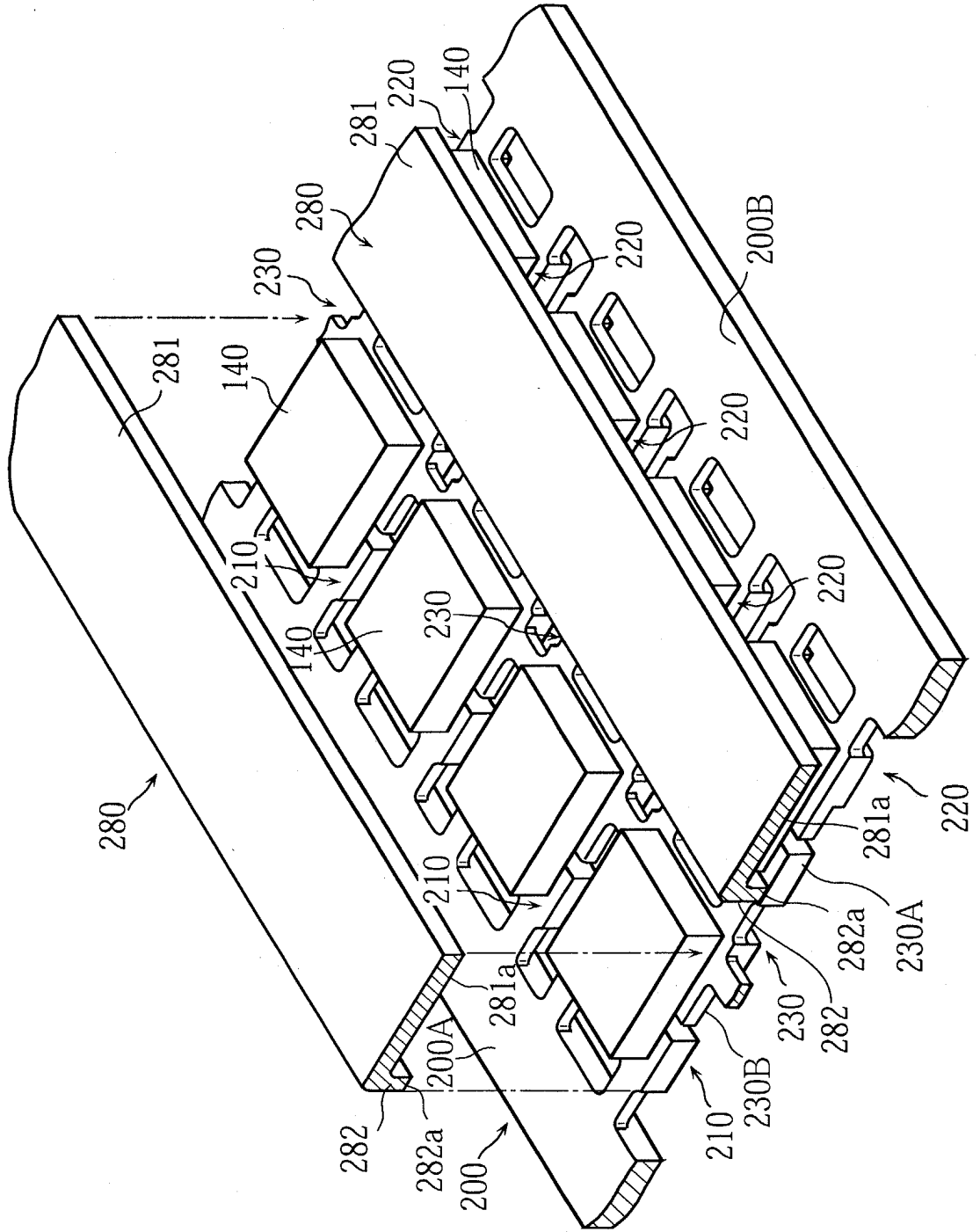


FIG. 8

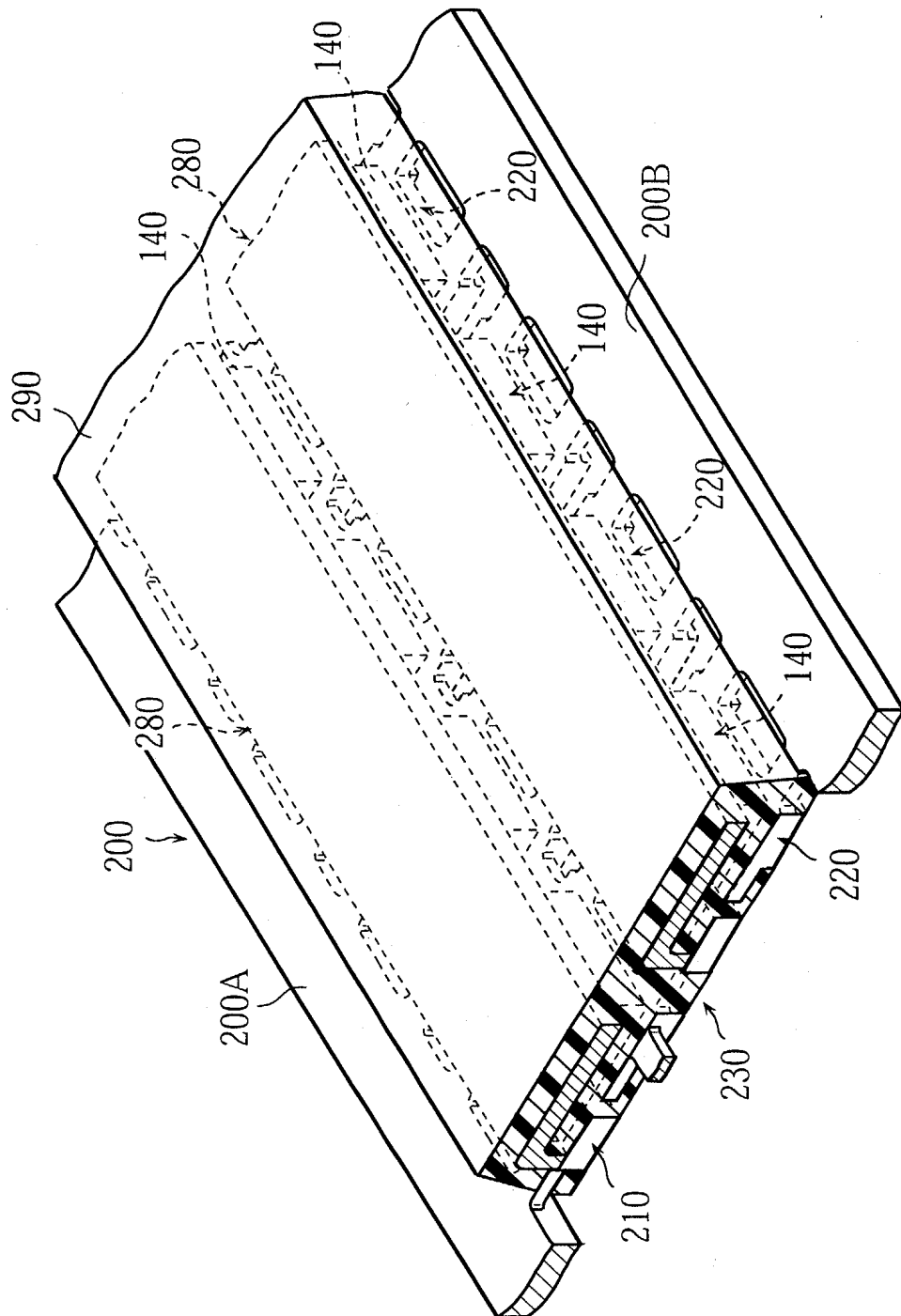


FIG. 9

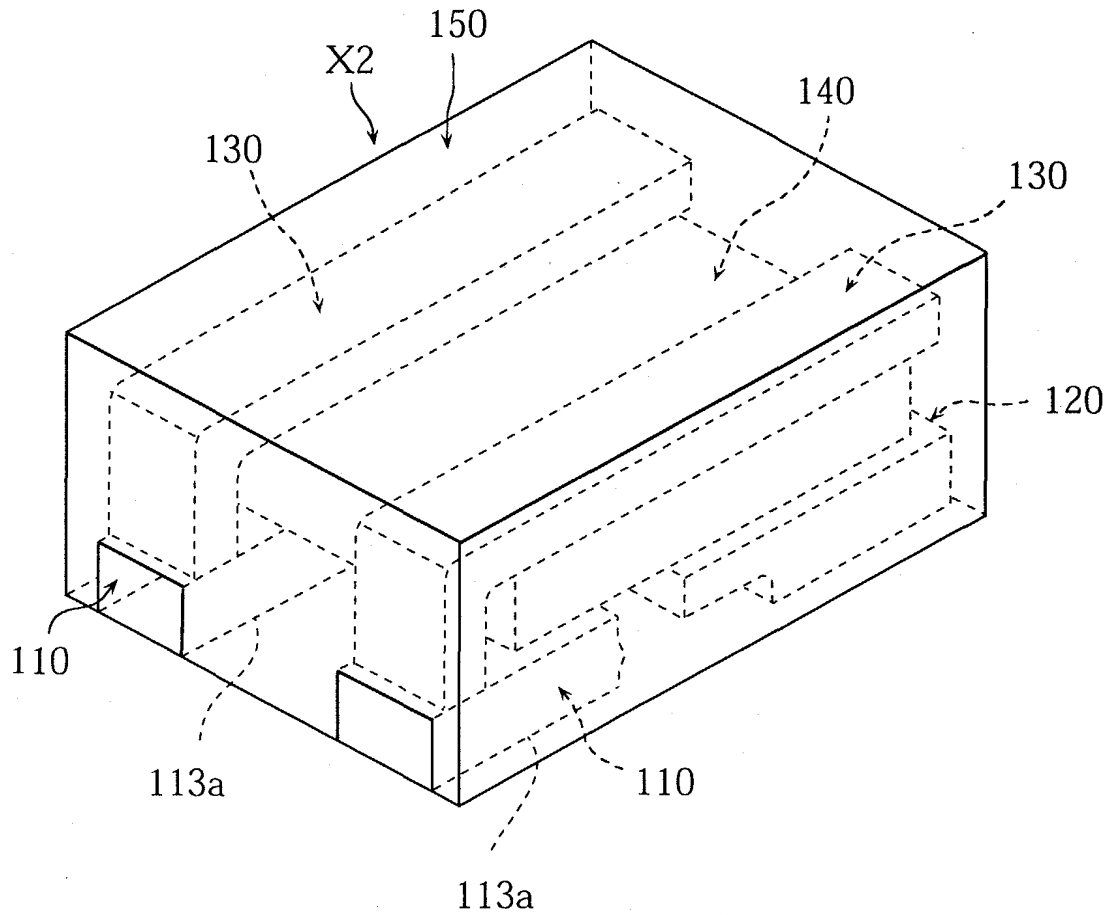


FIG. 10

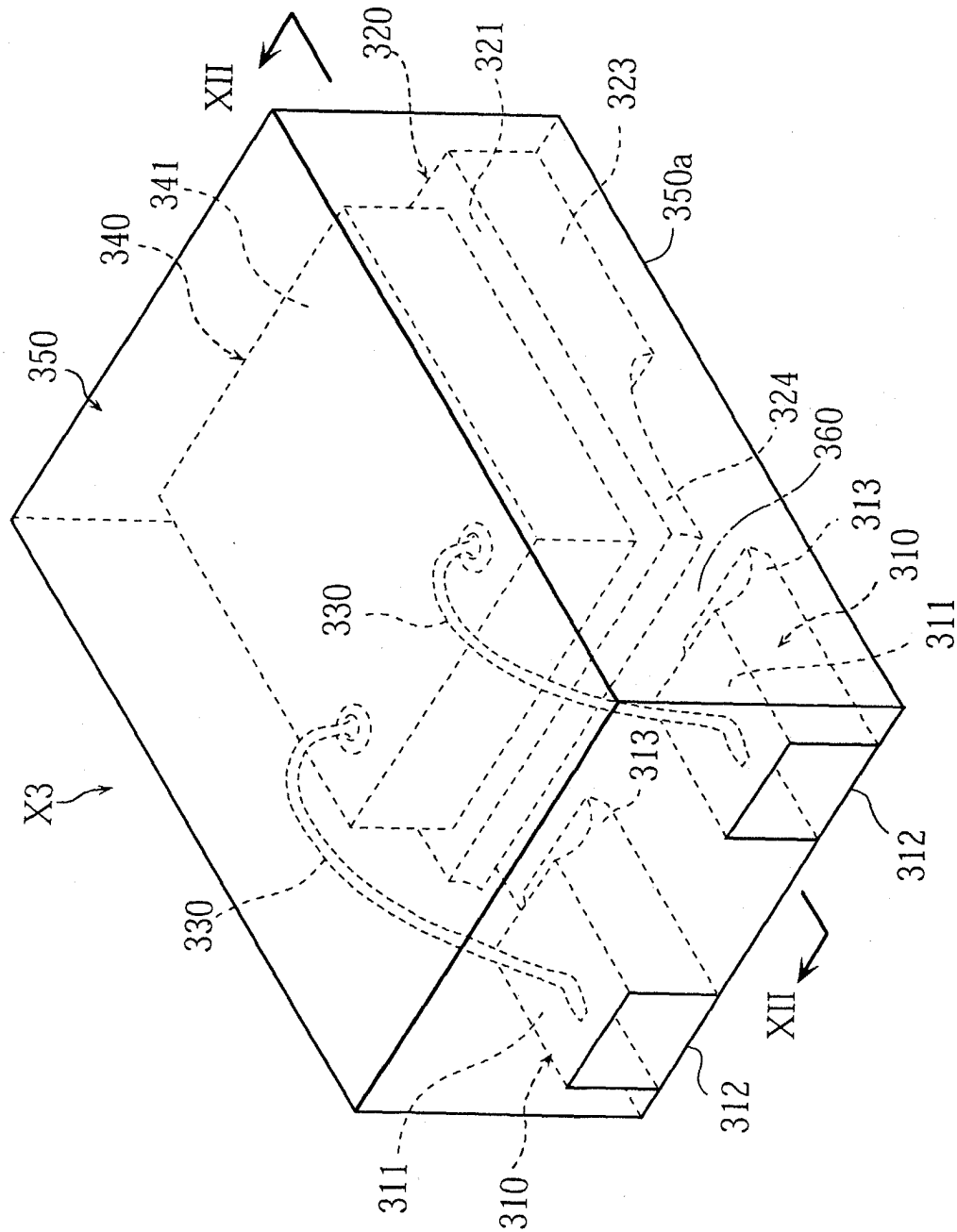


FIG. 12

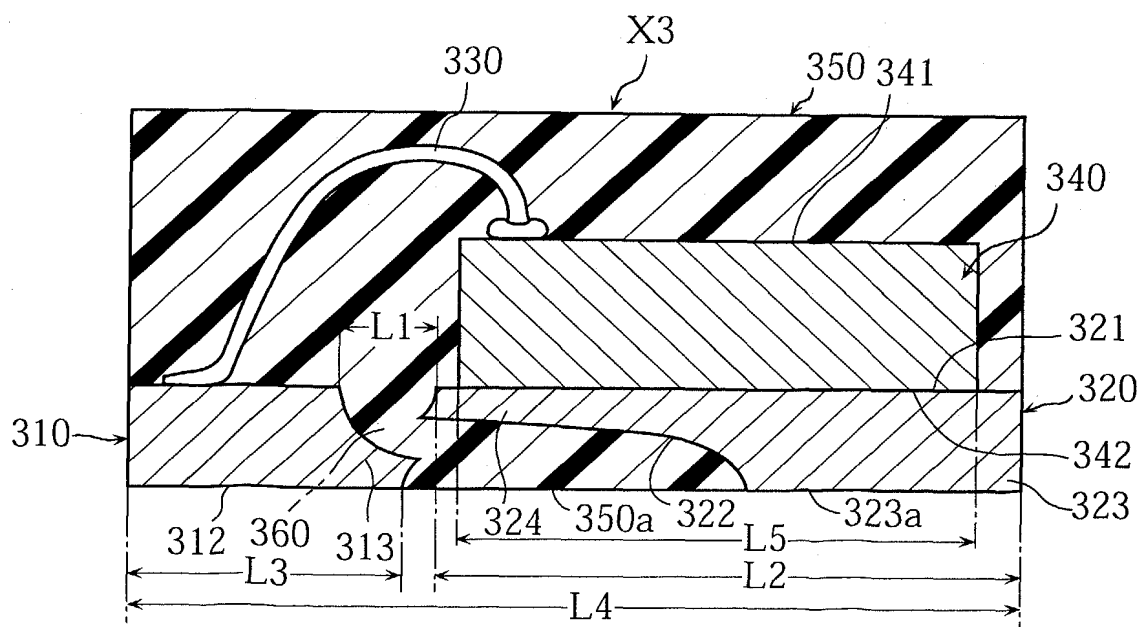


FIG. 13

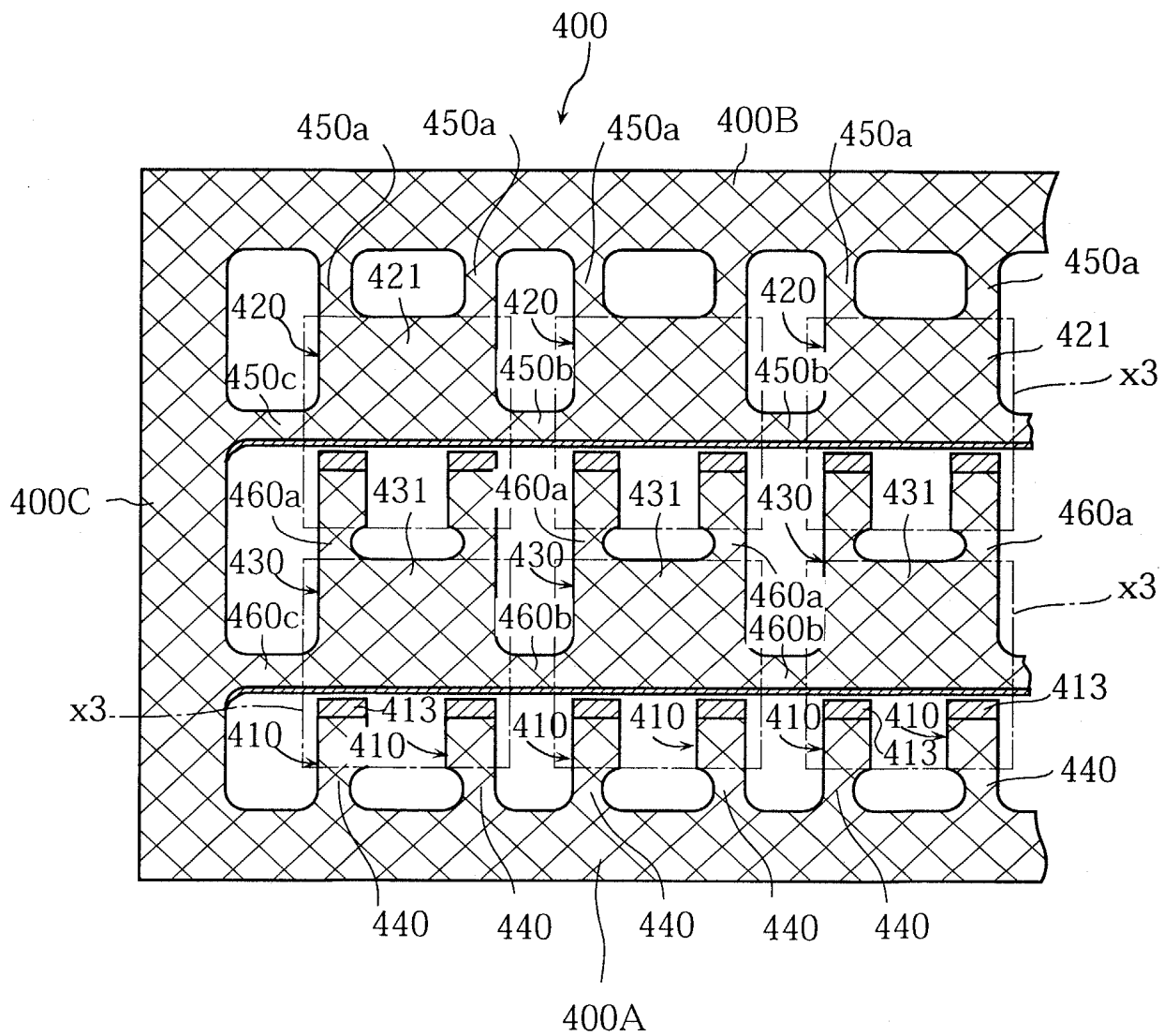


FIG. 14

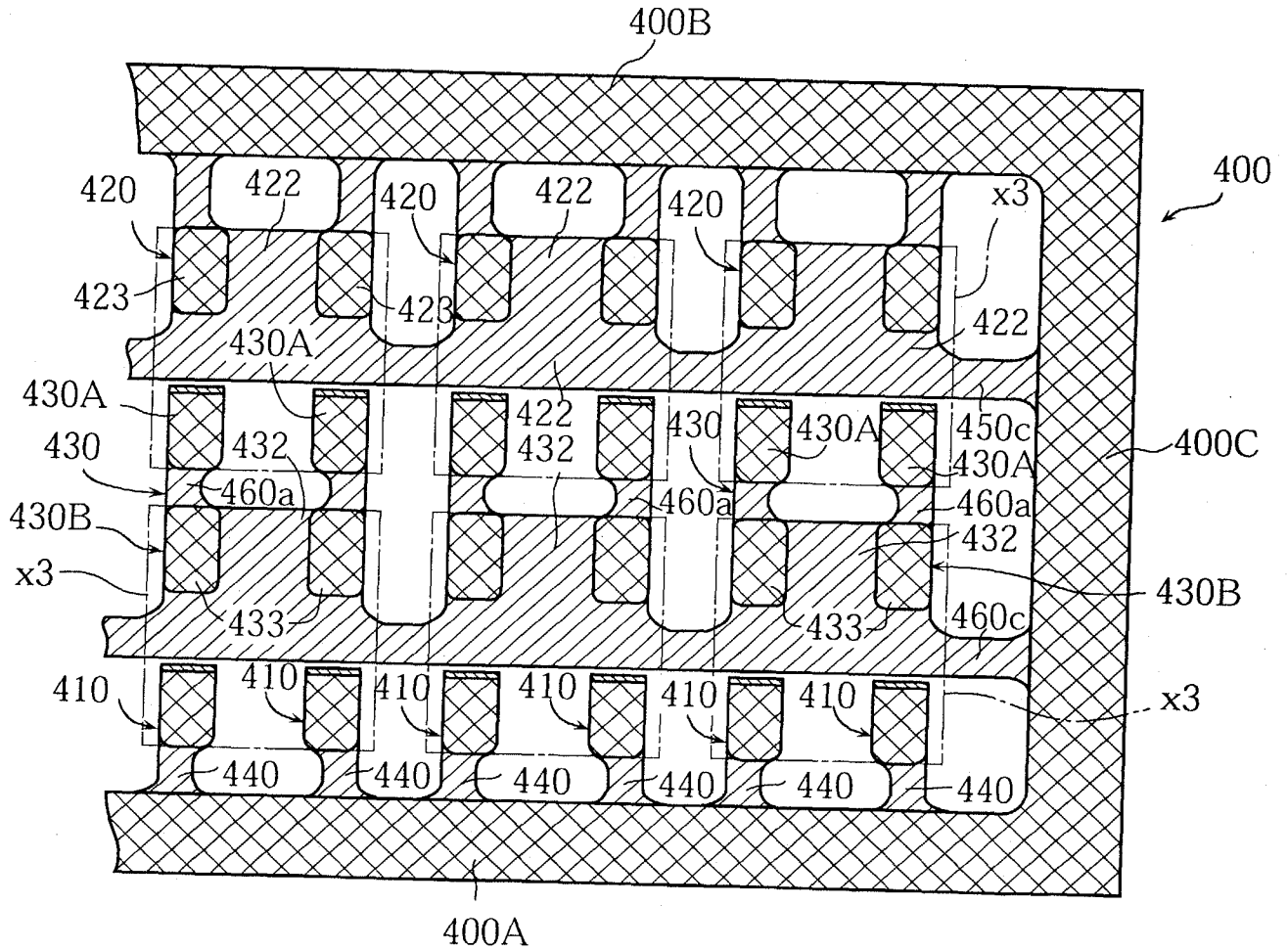


FIG. 15A

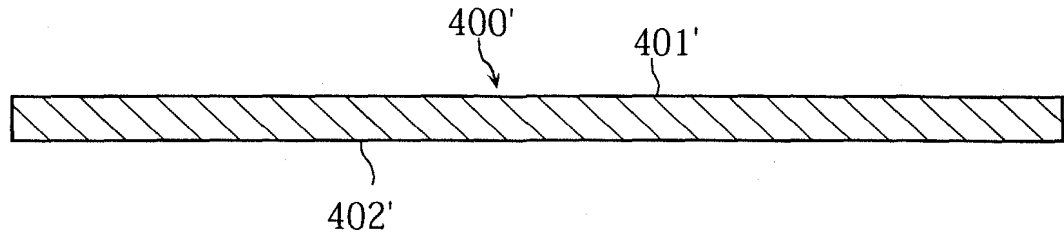


FIG. 15B

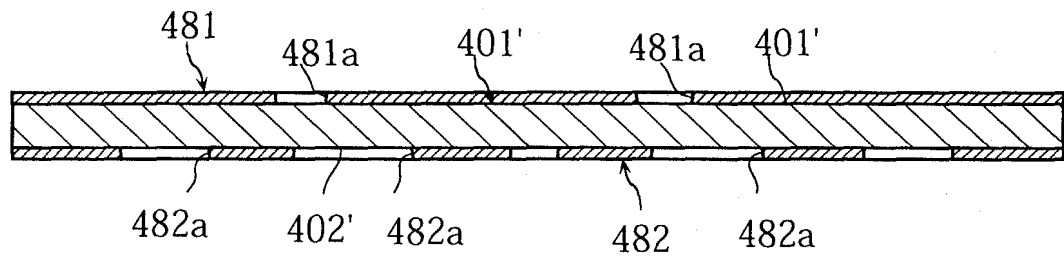


FIG. 15C

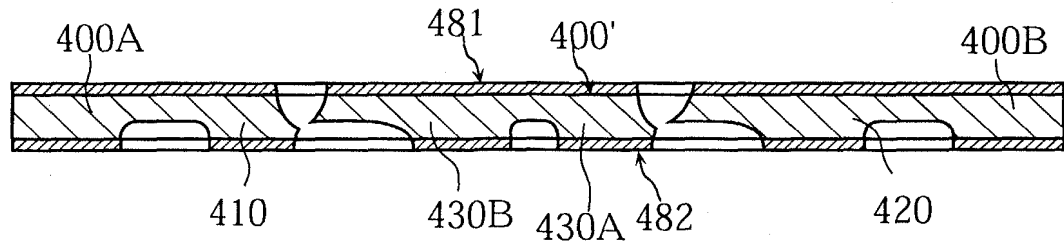


FIG. 15D

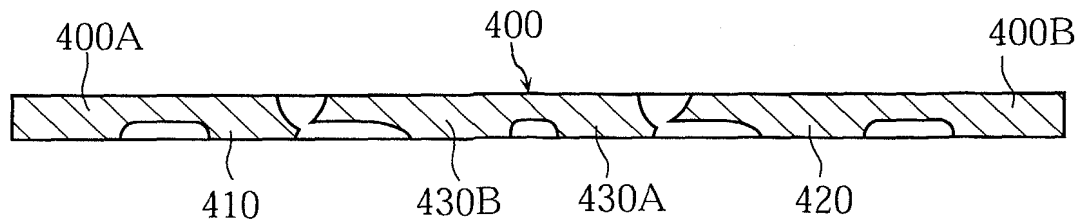


FIG. 16

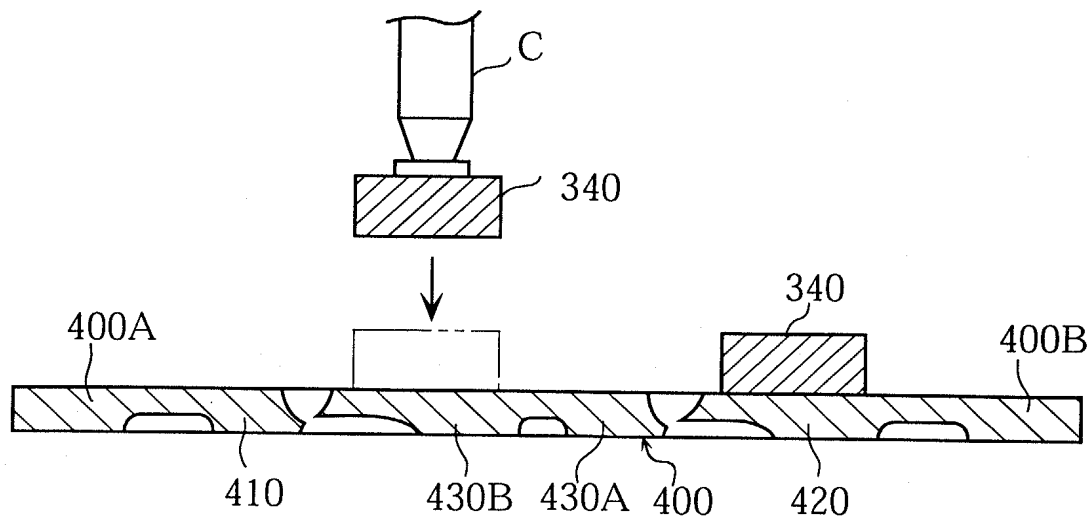


FIG. 17

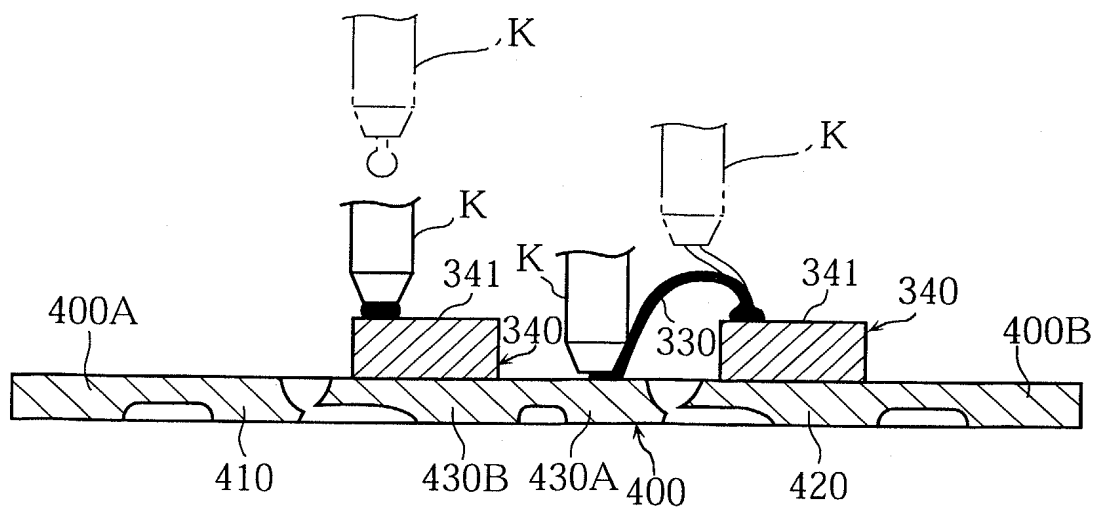
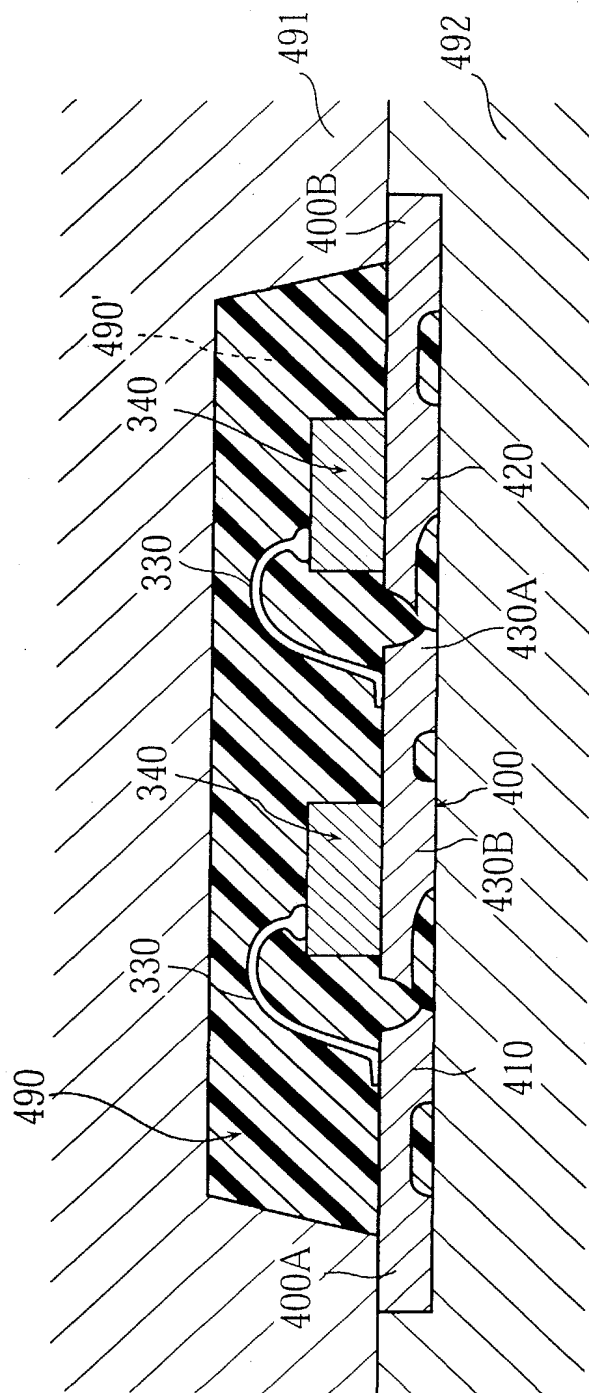


FIG. 18



16/36

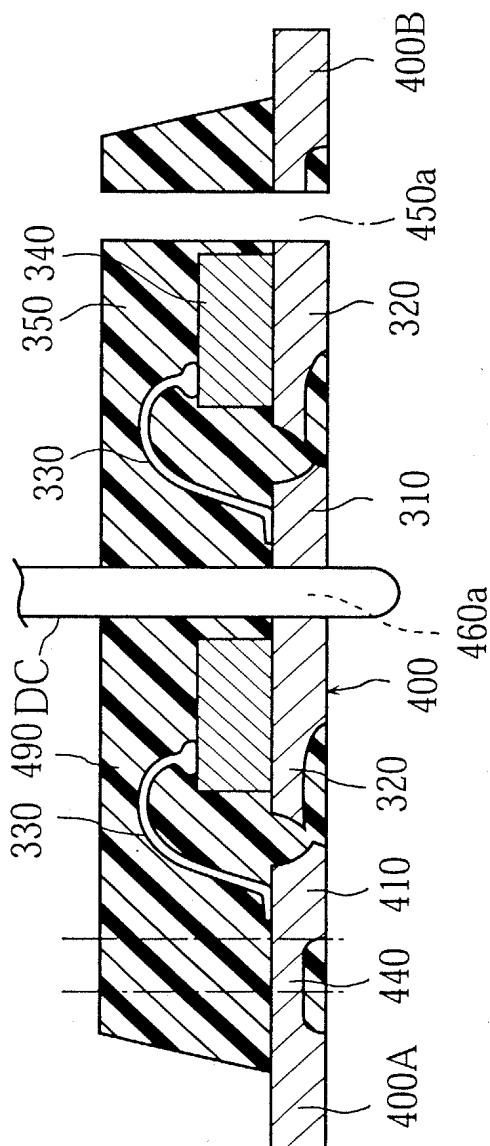


FIG. 20

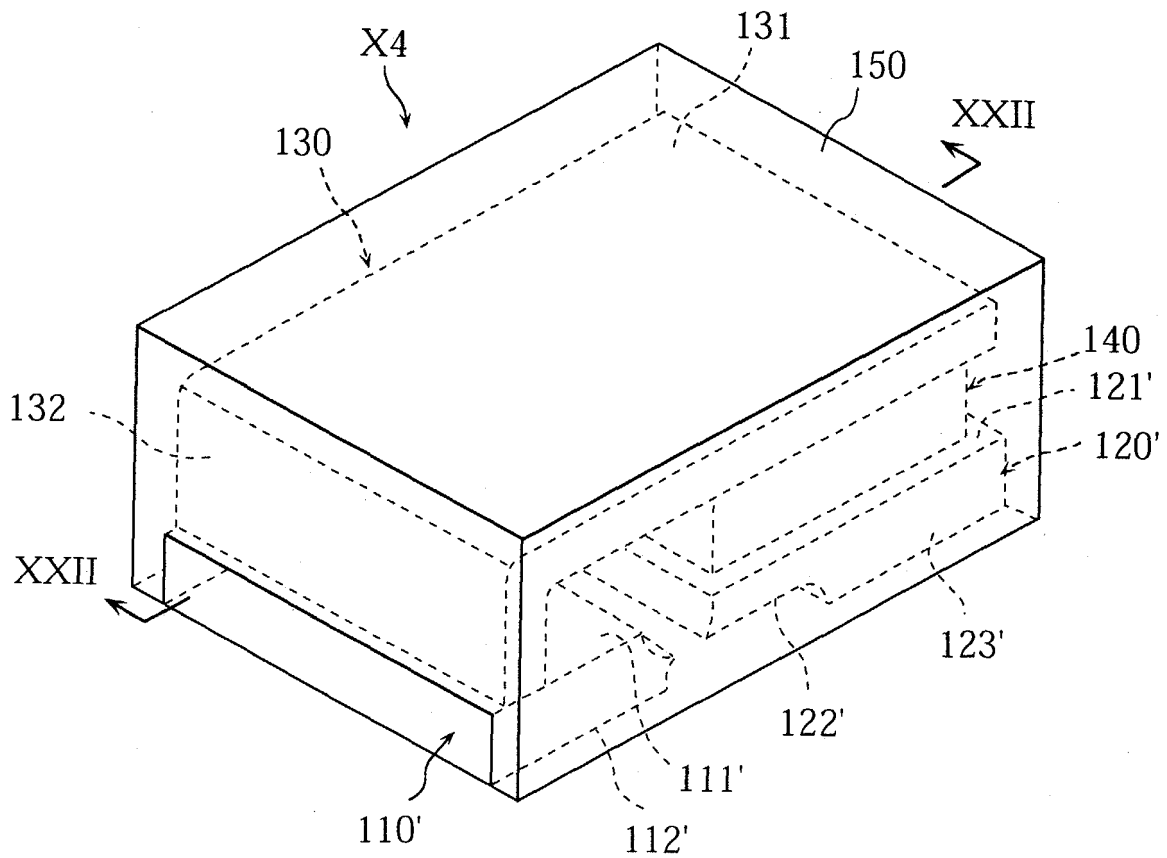


FIG. 22

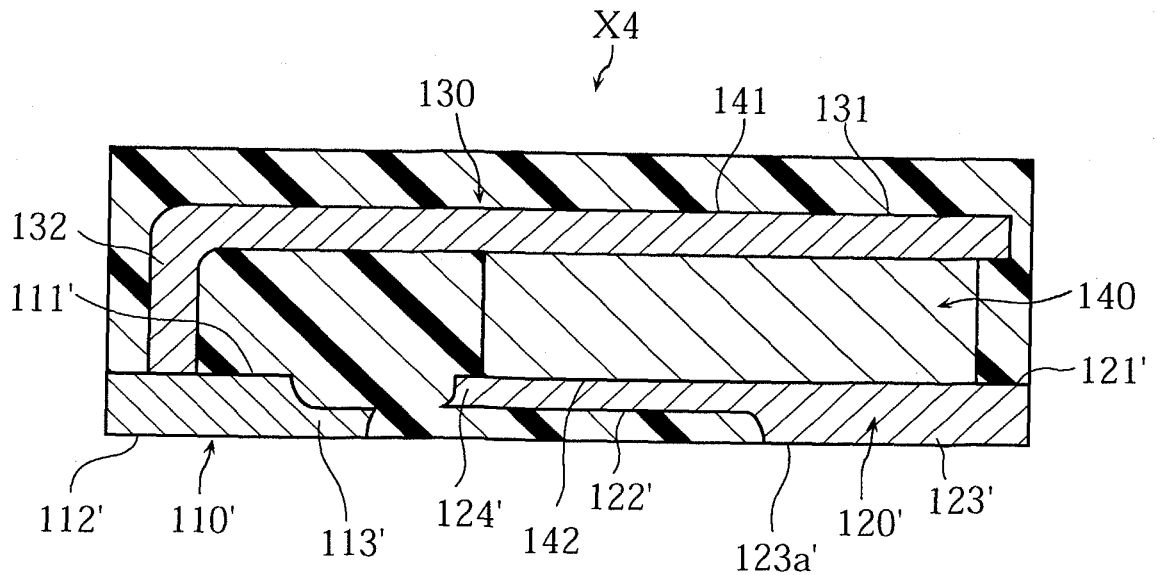


FIG. 23

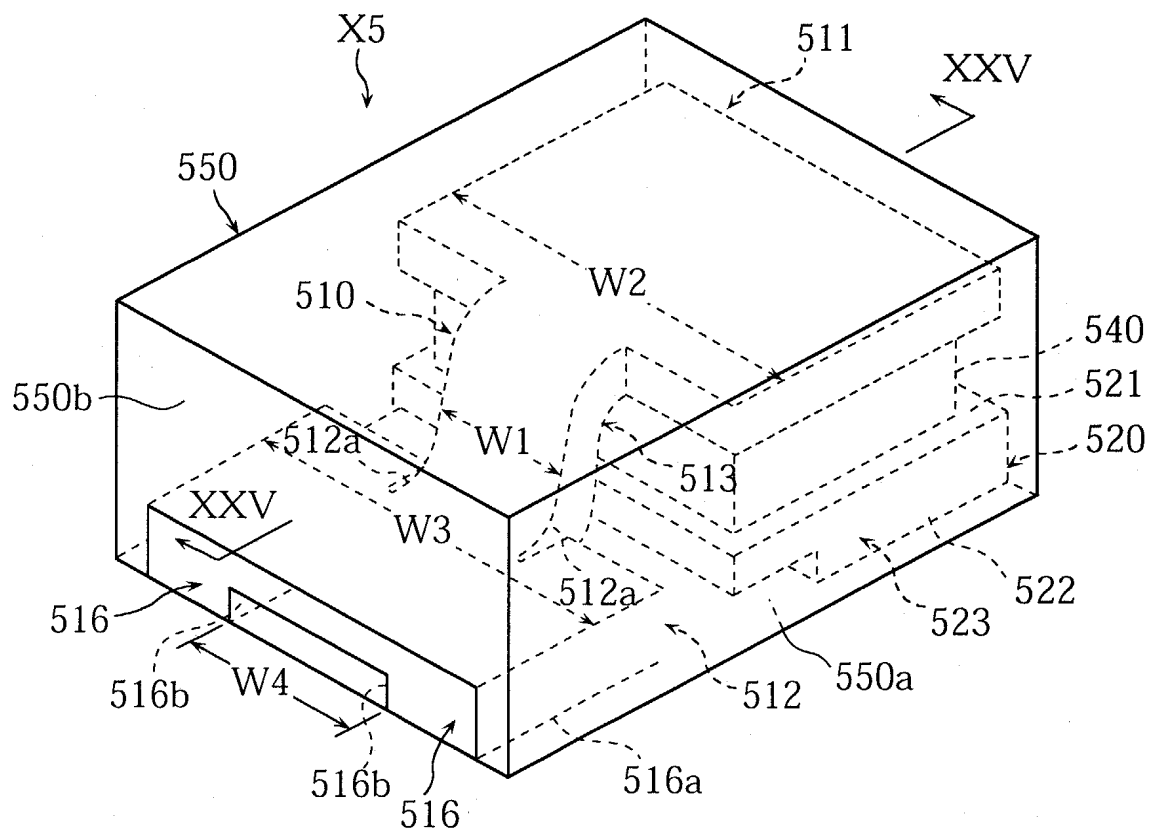


FIG. 24

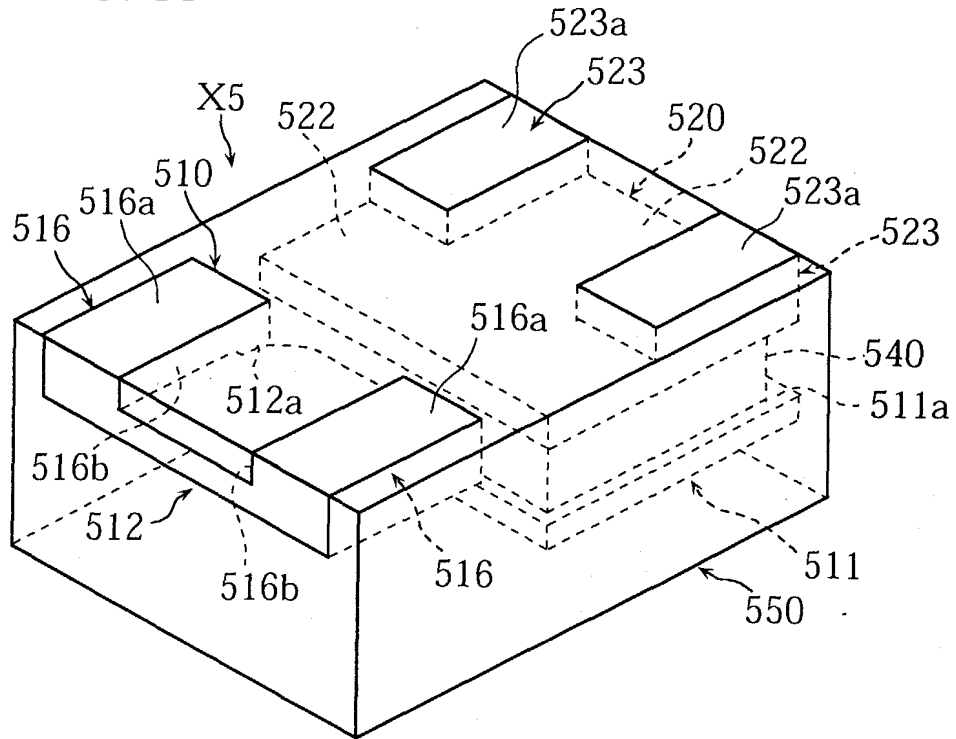


FIG. 25

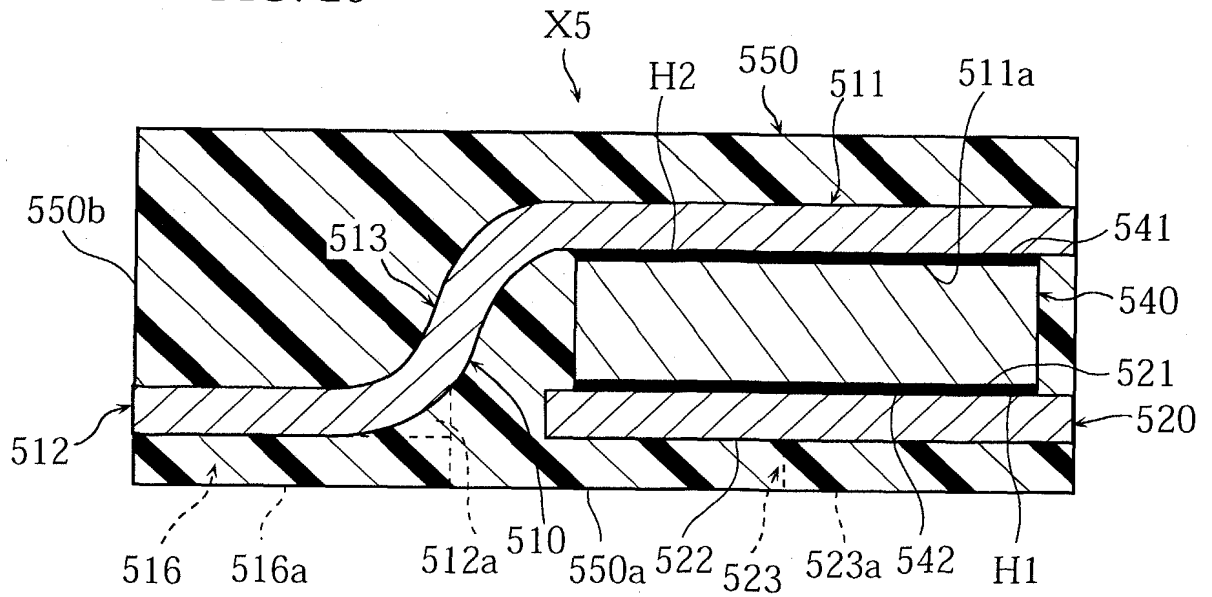


FIG. 27

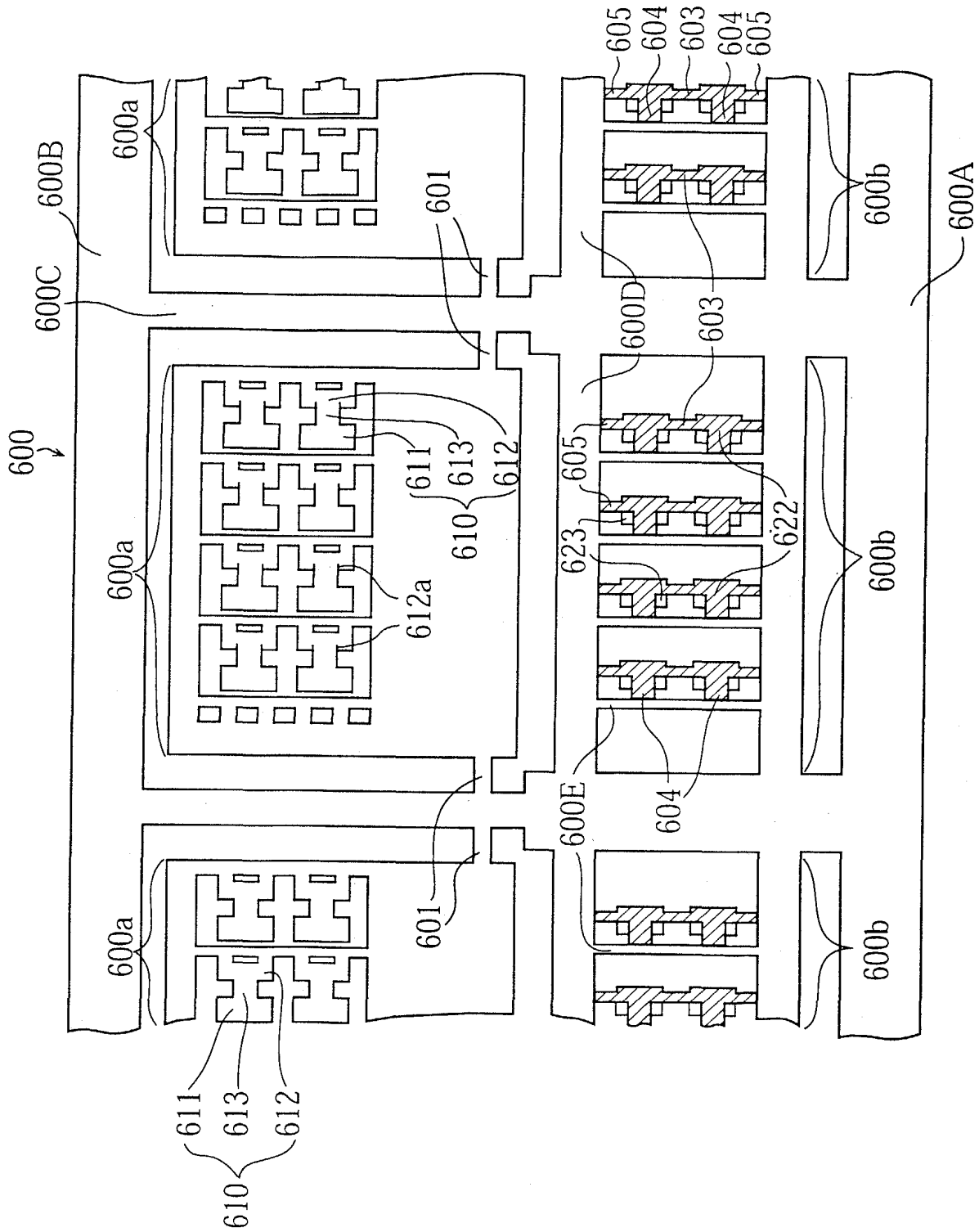


FIG. 6 is a cross-sectional view of a semiconductor device 600. The device includes a substrate 611 with a conductive layer 610. The conductive layer 610 has three U-shaped regions 612a, each containing a conductive plug 612. The regions are separated by insulating regions 613. A conductive layer 616 is on top of the plugs 612.

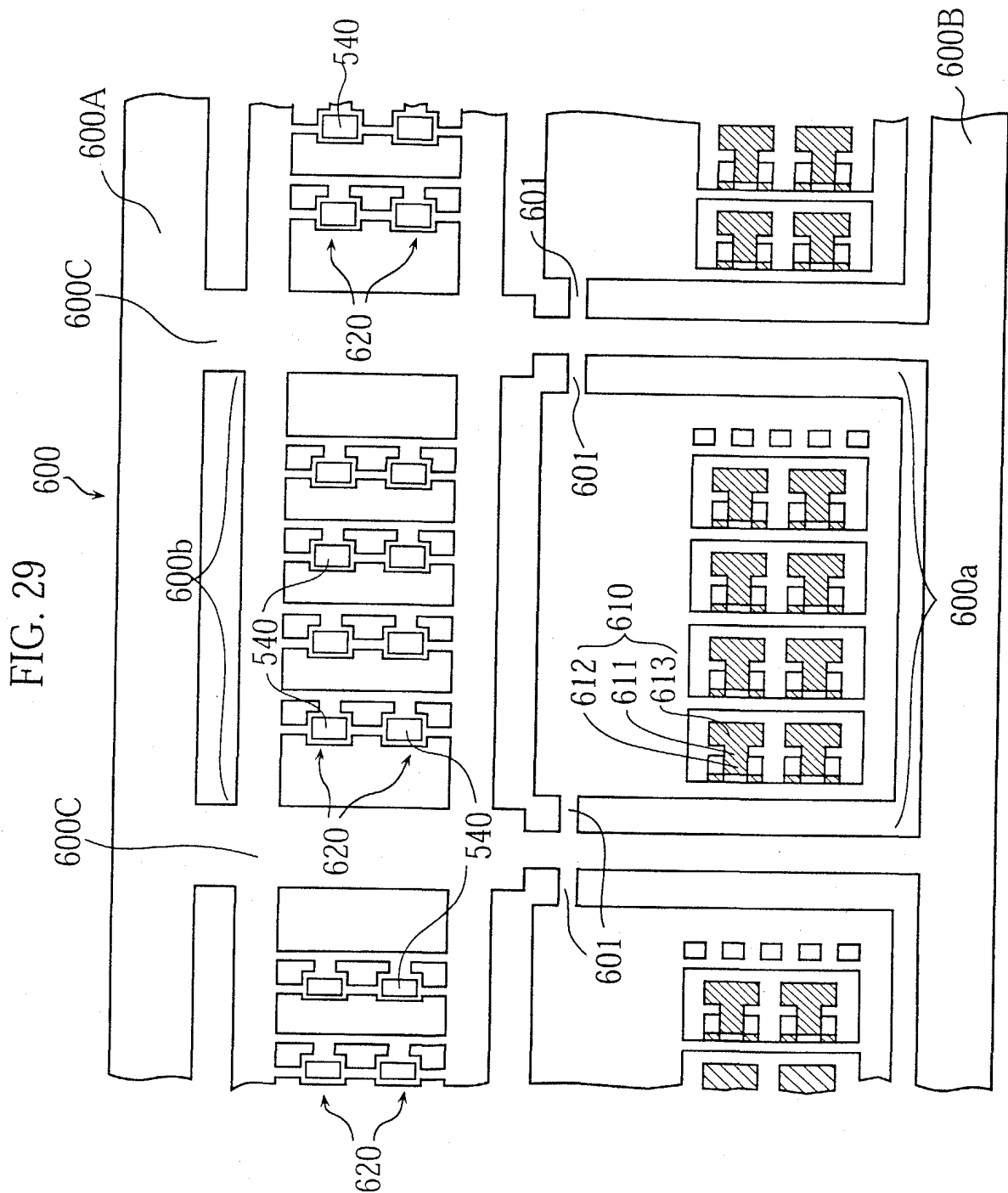


FIG. 30

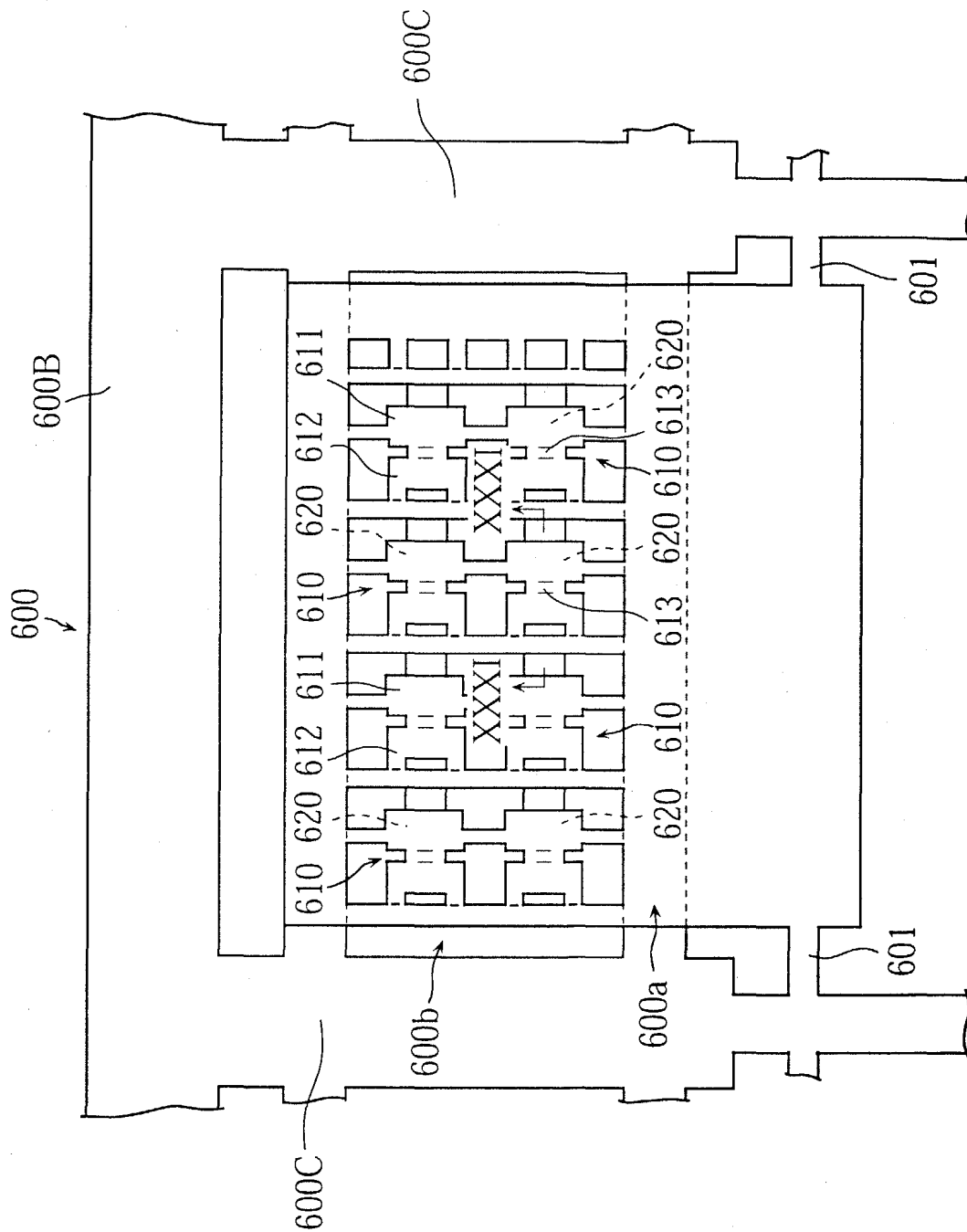


FIG. 32

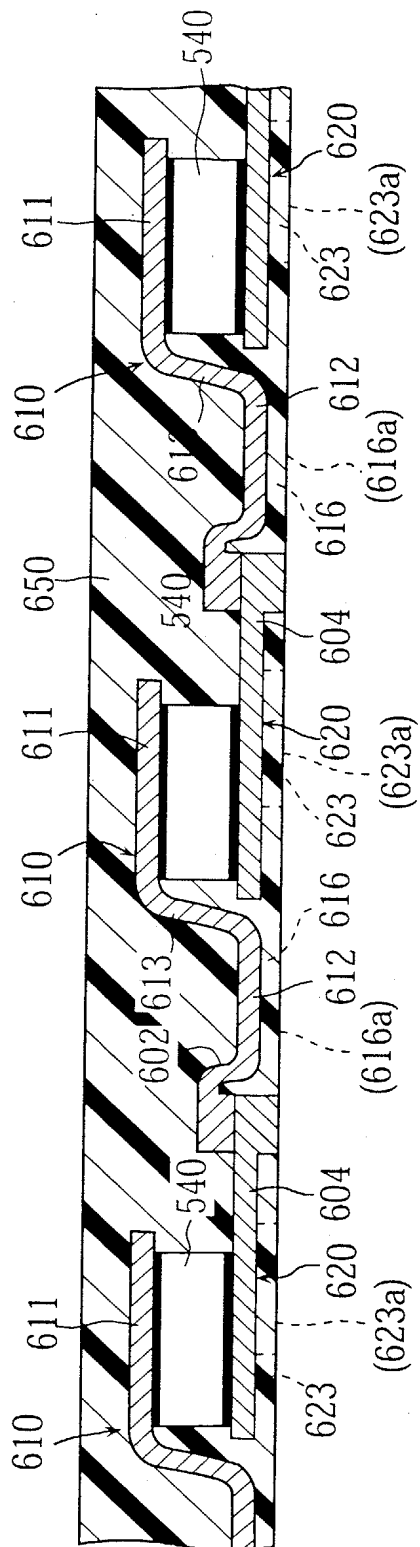


FIG. 33

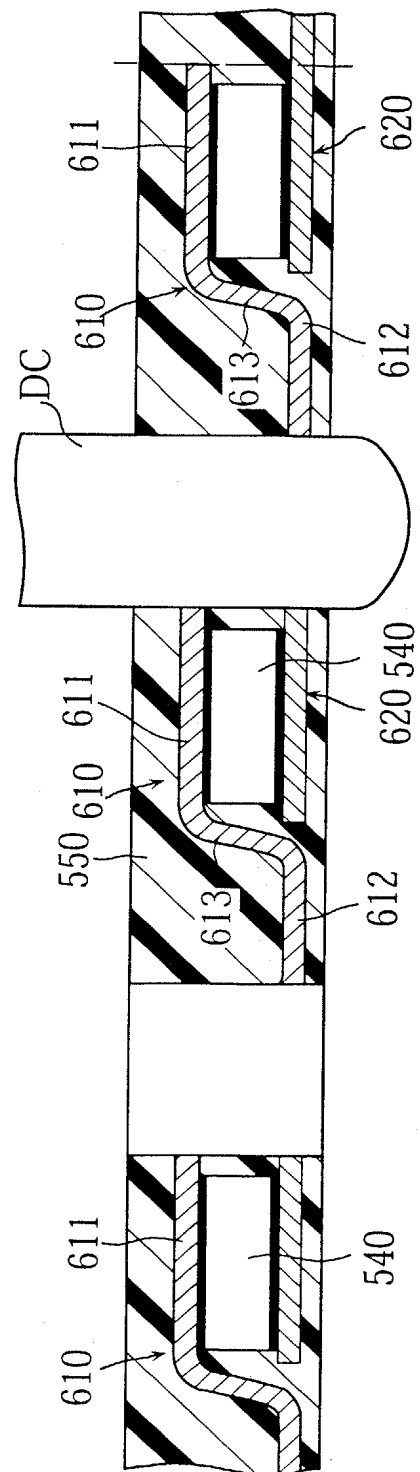


FIG. 34

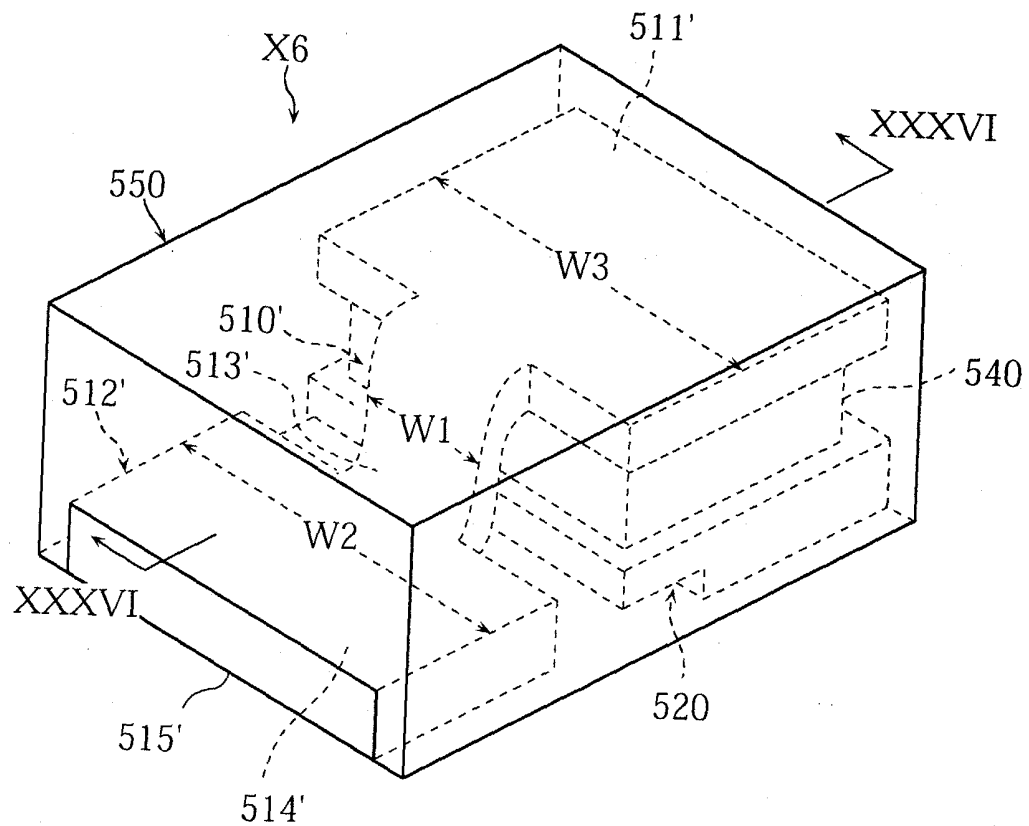


FIG. 35

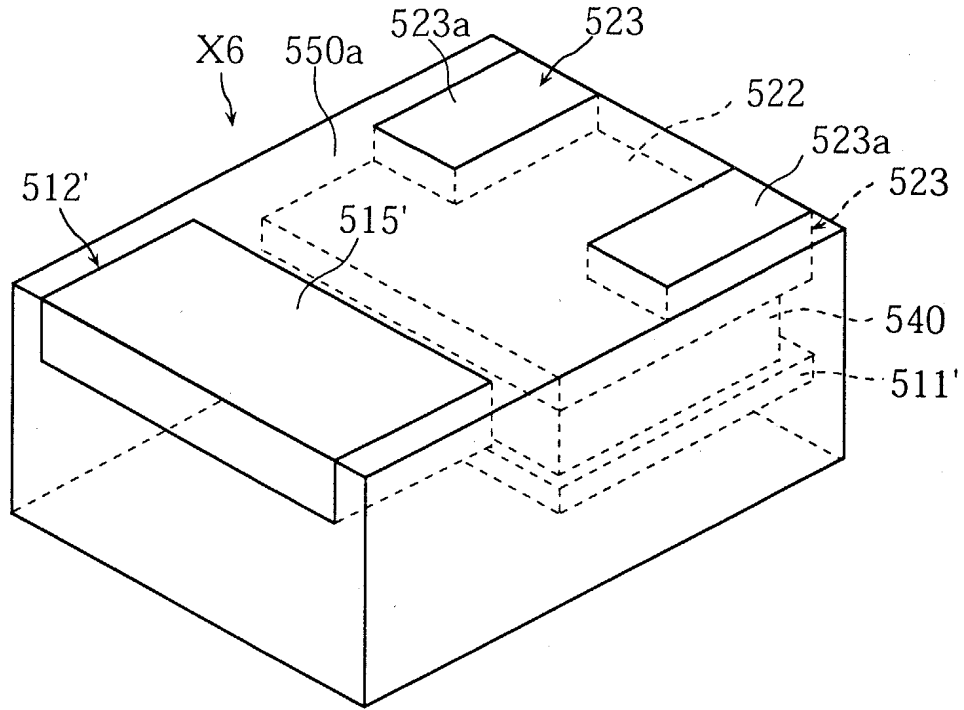


FIG. 36

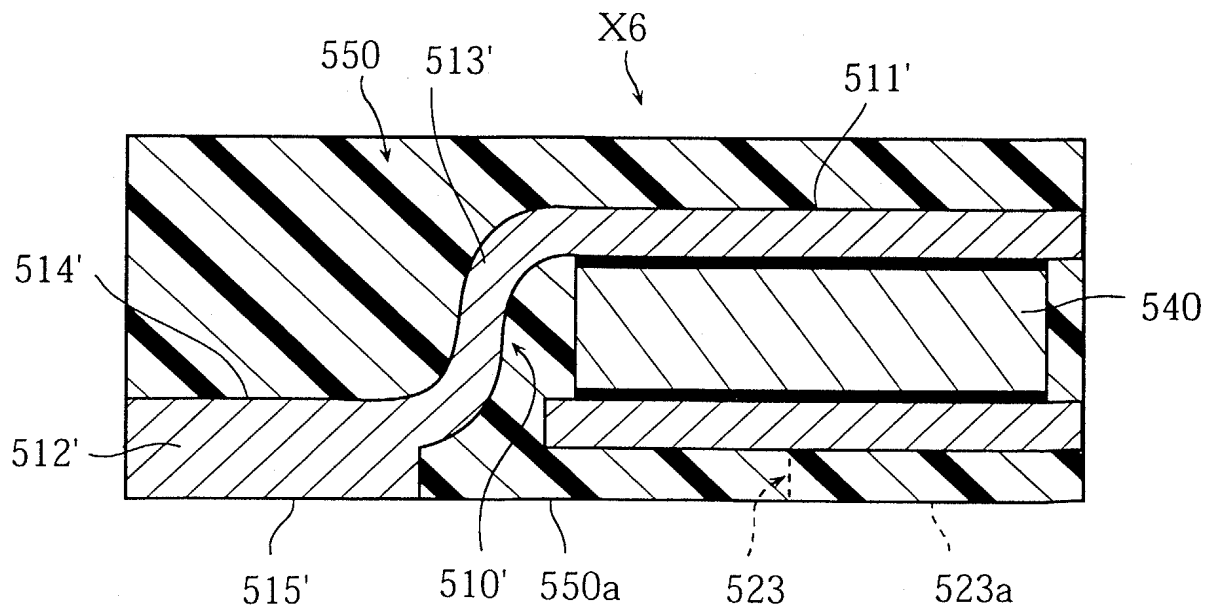


FIG. 37

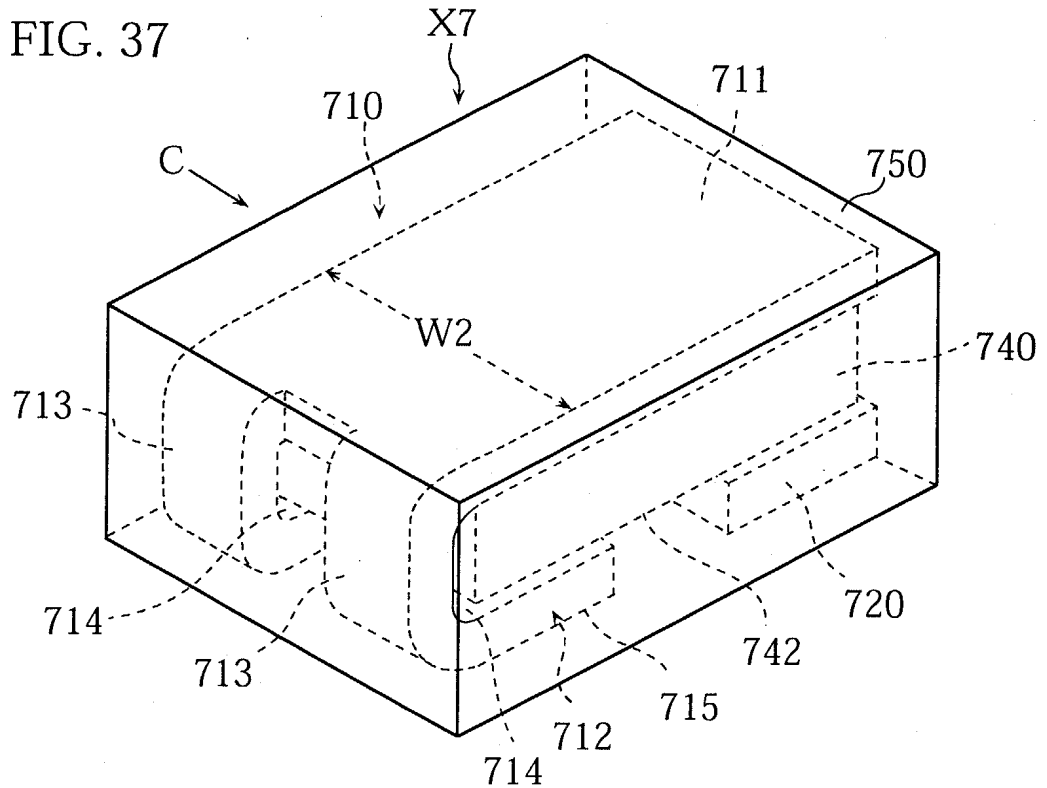


FIG. 38

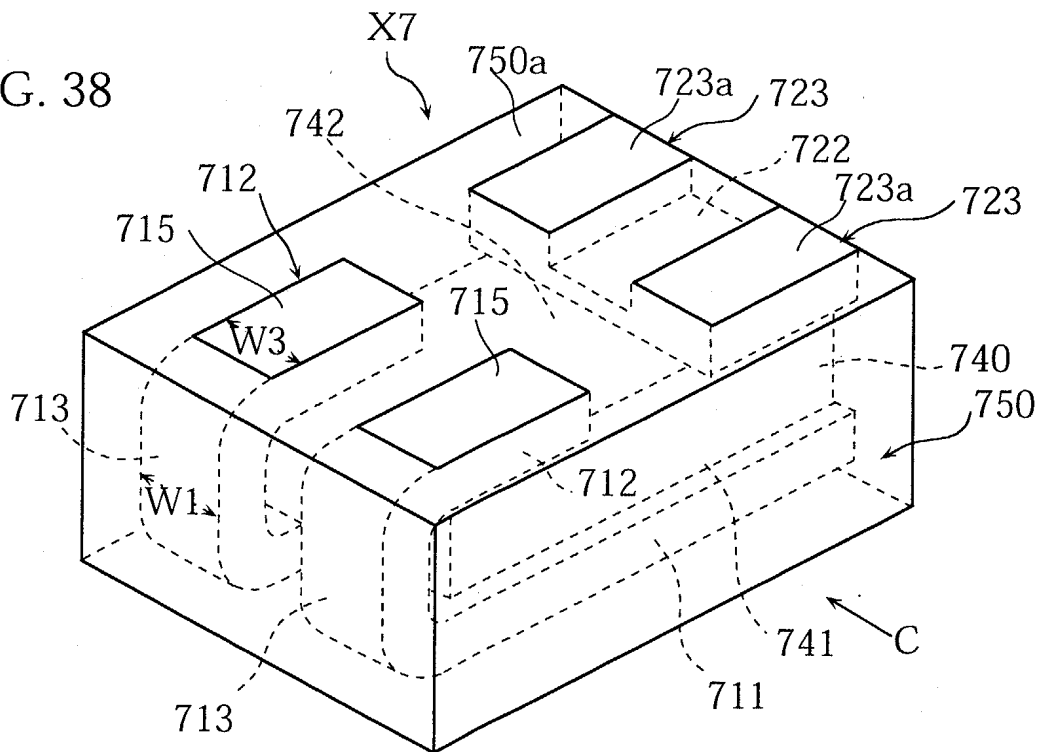


FIG. 39

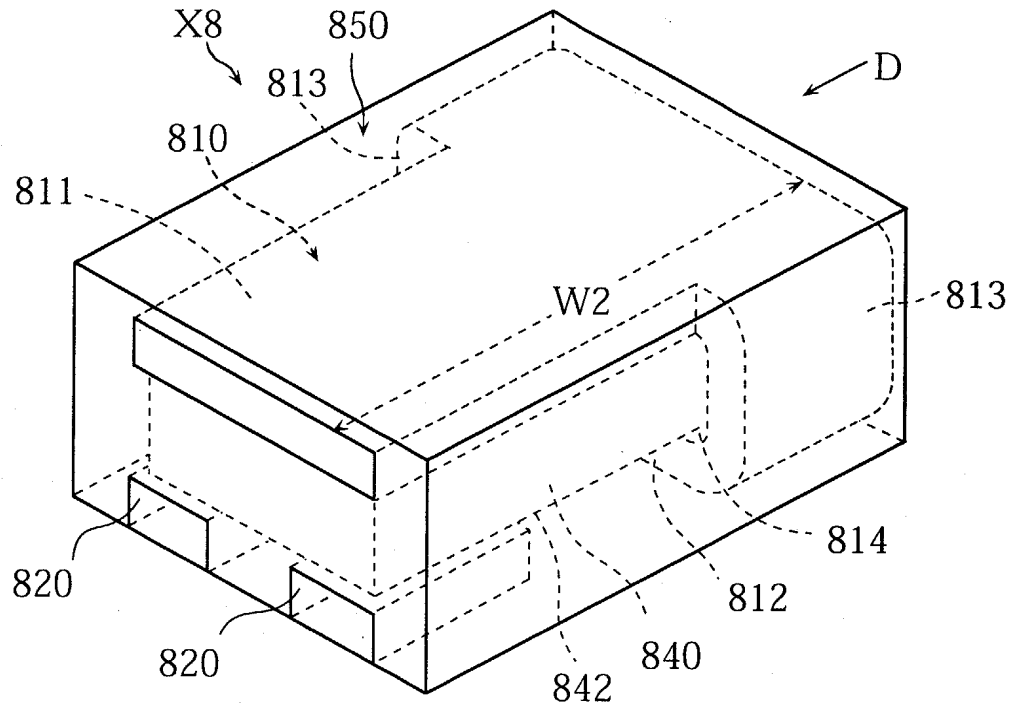


FIG. 40

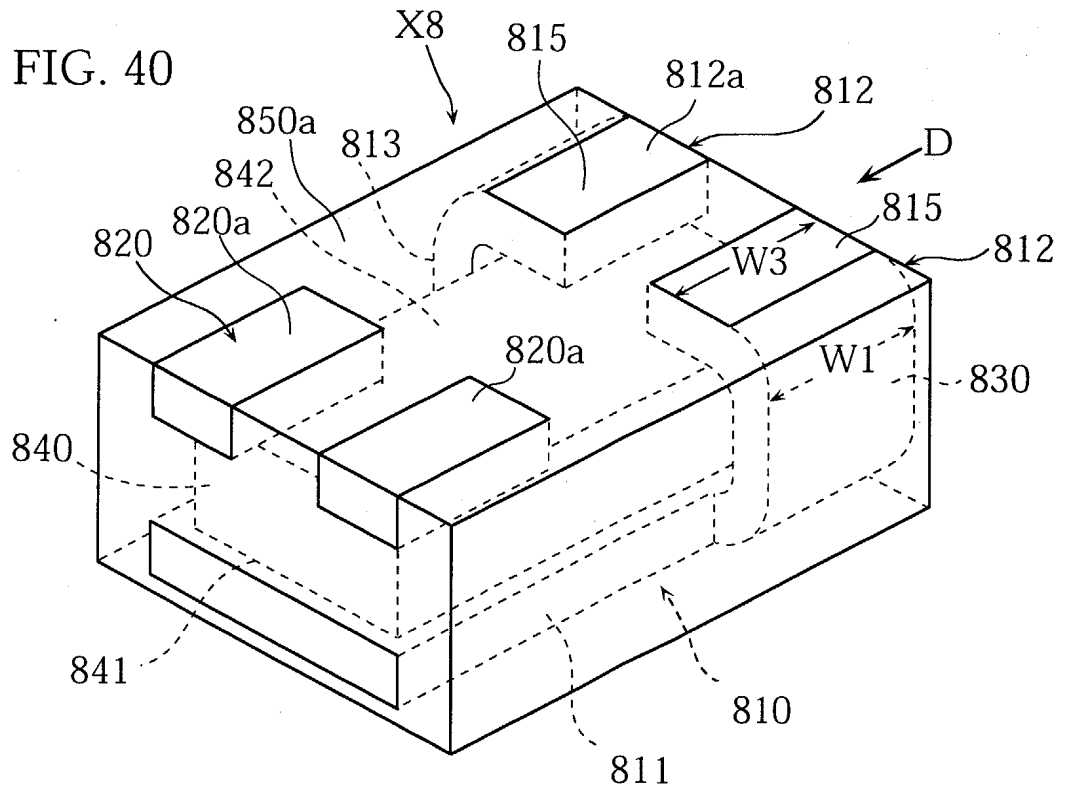


FIG. 41

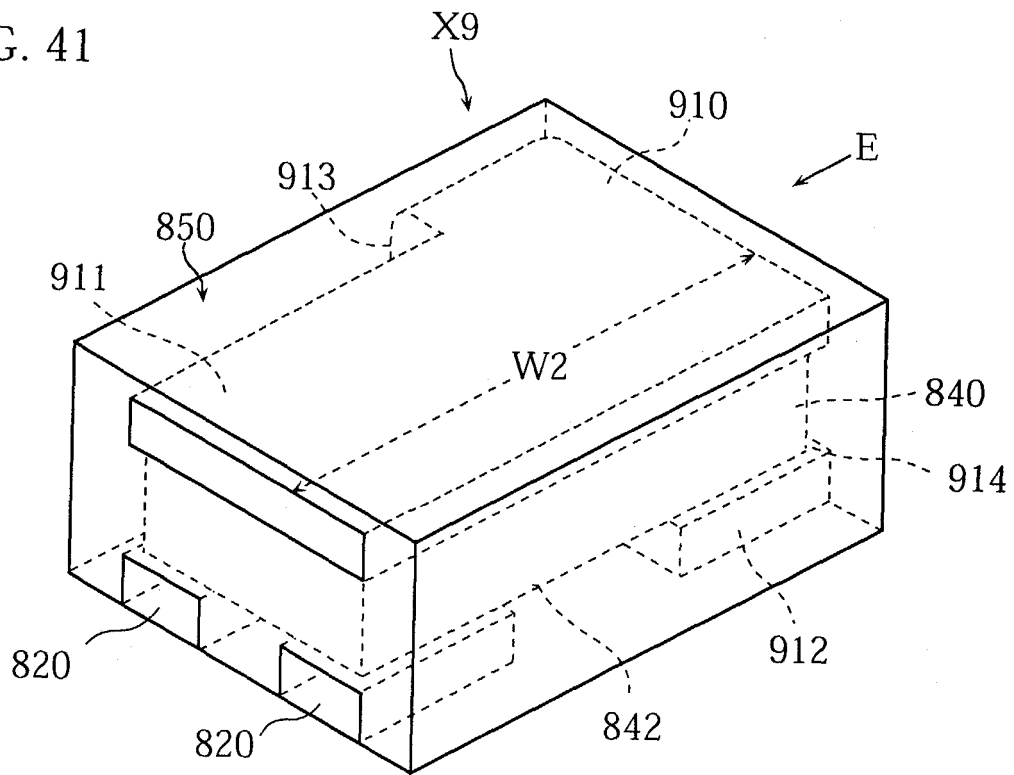
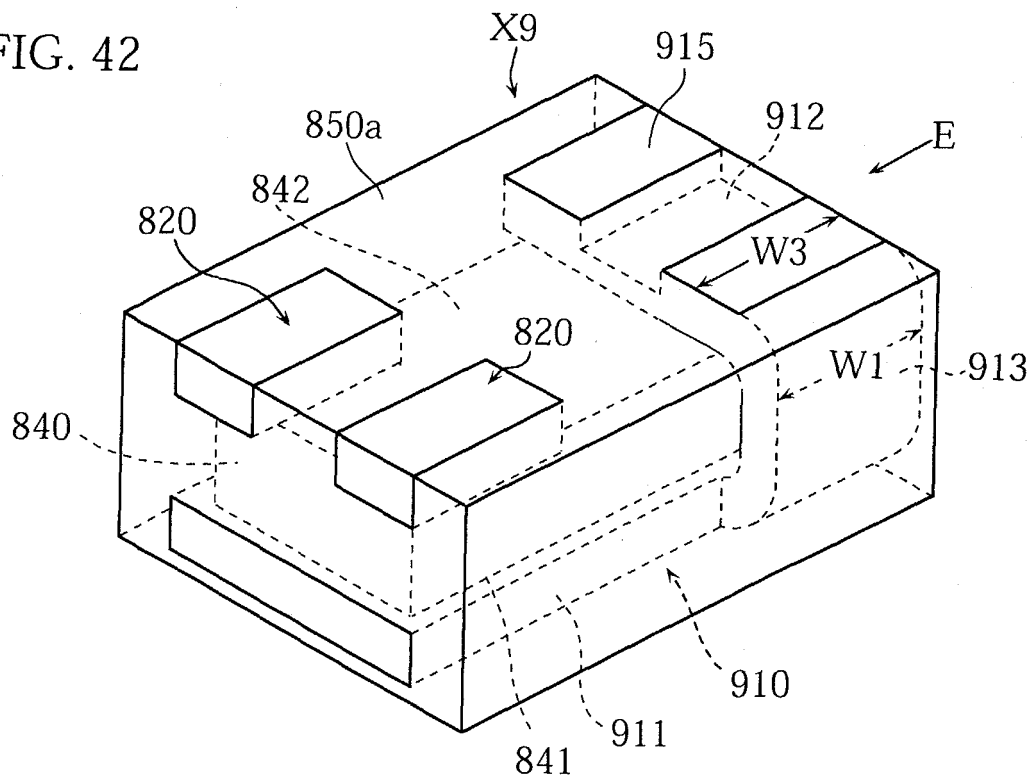


FIG. 42



[illegible][illegible]

FIG. 46
PRIOR ART

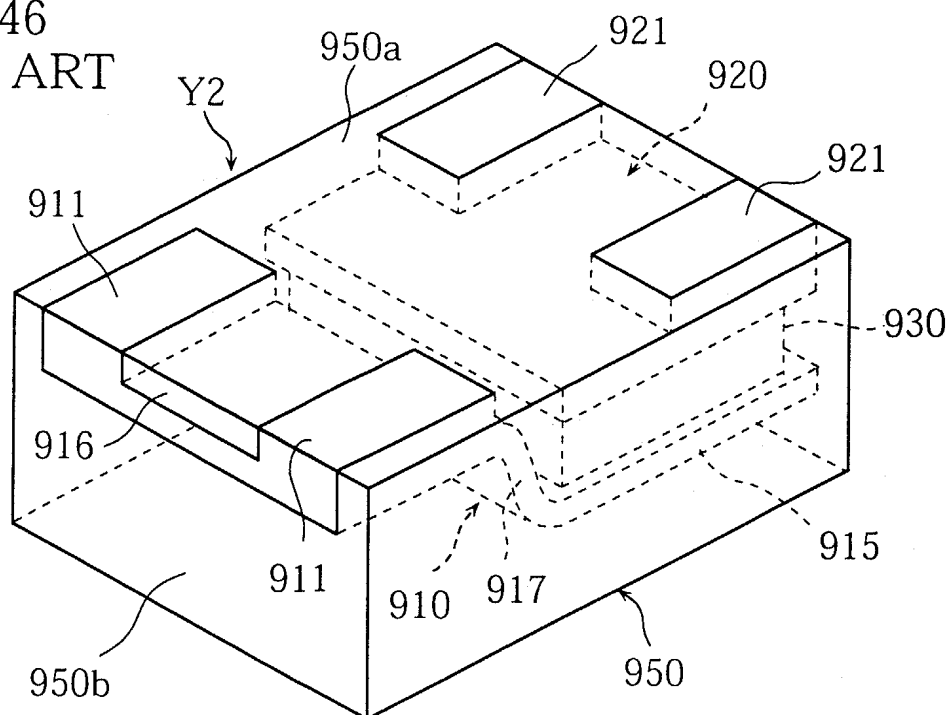
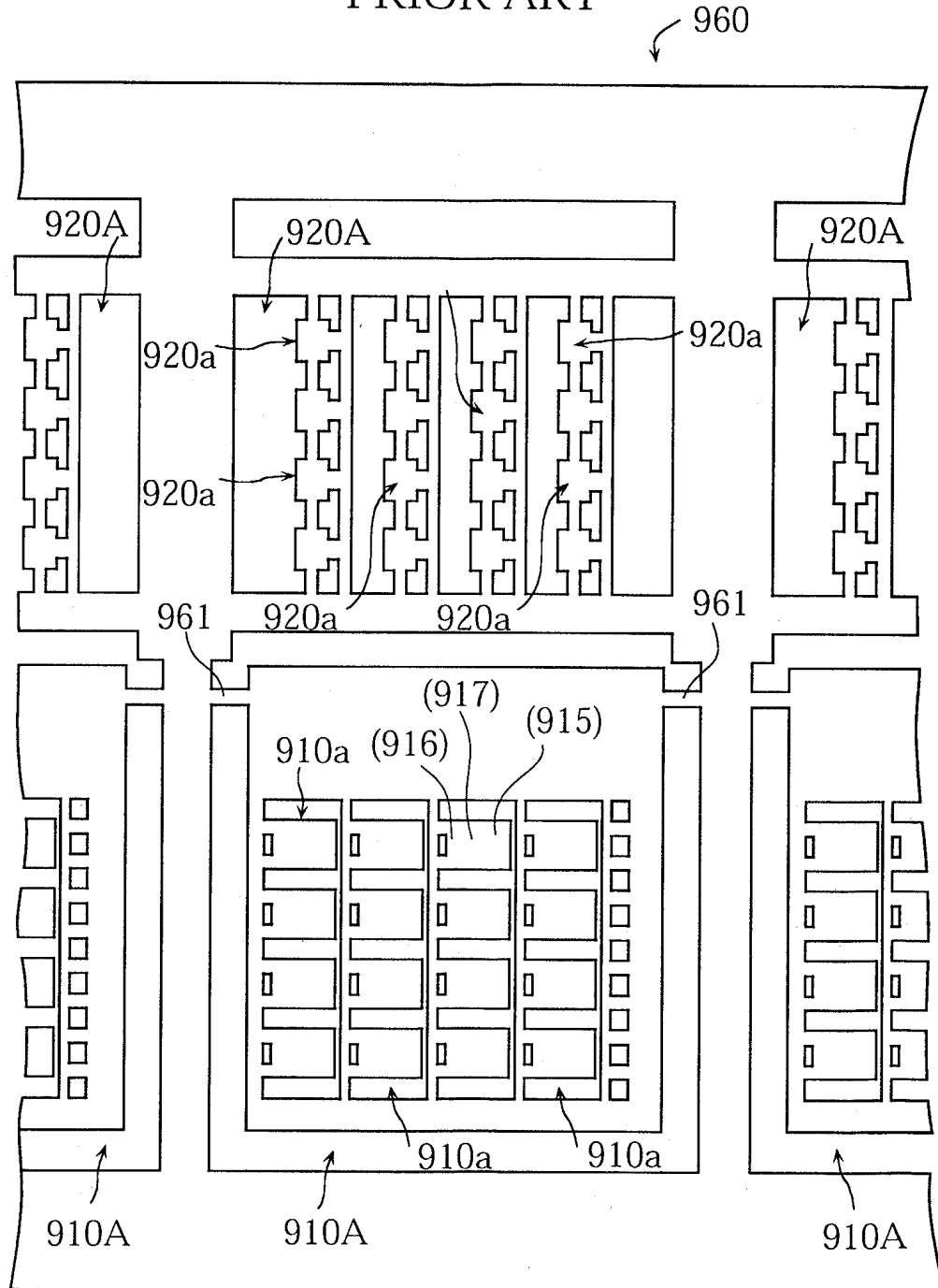


FIG. 47
PRIOR ART



36/36

